AMENDMENT TO THE CLAIMS

Please amend the presently pending claims as follows:

1. (Currently Amended) A parallel turbo decoder ~~routing multiplexer system~~ comprising:

an interleaver memory comprising n interleaver memory outputs;

a routing multiplexer, comprising:

n multiplexer inputs coupled to the n interleaver memory outputs;

p multiplexer outputs based on a selected permutation of the n ~~interleaver memory~~ multiplexer inputs, where p and n are integer variables and $n \geq p$~~, the multiplexer system comprising:~~ ; and

a plurality of modules arranged in an array of interconnected rows, each module having first and second inputs, first and second outputs and a control input and arranged to supply signals at the first and second inputs to the first and second outputs in a direct or transposed order based on a value of a control bit at the control input, the array comprising a first row formed by a first group of p/2 of the modules ~~being~~ of which the first and second inputs are each coupled to a respective one [[p]] of the n ~~interleaver memory~~ multiplexer inputs and a last row formed by a second group of p/2 of the modules ~~being~~ of which the first and second outputs are each coupled to a respective one of the p multiplexer outputs; and

a memory containing a plurality of control bit tables each containing a plurality of control bits in an arrangement based on a respective permutation, the memory being responsive to the selected permutation to supply the plurality of control bits of the control bit table that corresponds to the selected permutation to ~~the~~ respective control inputs ~~of respective ones~~ of the modules.

2. (Currently Amended) The ~~multiplexer system~~ parallel turbo decoder of claim 1, wherein ~~the modules are arranged in an array of rows, and~~ each control bit table contains rows each

containing a plurality of the control bits, the memory supplying a j-th bit at an i-th row of a selected control bit table to the corresponding j-th module of the i-th row of the array.

3. (Currently Amended) The ~~multiplexer system~~ parallel turbo decoder of claim 2, wherein there are at least $(2k-1)\times 2^{k-1}$ modules and at least $(2k-1)\times 2^{k-1}$ control bits and the array of modules and each control bit table has 2k-1 rows, where $p=2^k$ and $k>0$.

4. (Currently Amended) The ~~multiplexer system~~ parallel turbo decoder of claim 1, wherein there are at least $(2k-1)\times 2^{k-1}$ modules and at least $(2k-1)\times 2^{k-1}$ bits, where $p=2^k$ and $k>0$.

5. (Currently Amended) An integrated circuit chip containing a circuit for mapping up to p memories for parallel turbo decoding, wherein p is an integer variable, the circuit comprising:

a routing multiplexer having:

a plurality of modules arranged in an array of interconnected rows, each module having first and second inputs, first and second outputs and a control input and arranged to supply signals at the first and second inputs to the first and second outputs in a direct or transposed order based on a value of a control bit at the control input, the array comprising a first row formed by a first group of p/2 of the modules, of which the first and second inputs are each coupled to a respective one of the memories, and a last row formed by a second group of p/2 of the modules, of which each of the first and second outputs form a respective map output, and

a permutation memory containing plurality of control bit tables each containing a plurality of the control bits in an arrangement based on a respective permutation~~,~~

~~map inputs coupling an output of each memory to respective ones of the first and second inputs of a first group of p/2 of the modules;~~

~~map outputs coupled to respective ones of the first and second outputs of a second group of p/2 of the modules~~; and

a permutation selection device coupled to the permutation memory for operating the permutation memory to select one of the control bit tables to supply the control bits of that table

to the control inputs of the modules.

6. (Currently Amended) The ~~mapping apparatus~~ integrated circuit chip of claim 5, wherein ~~the modules are arranged in an array of rows~~ each ~~containing~~ row contains p/2 modules, and each control bit table contains rows each containing p/2 control bits, the memory supplying a j-th bit at an i-th row of a selected control bit table to the corresponding j-th module of the i-th row of the array.

7. (Currently Amended) The ~~mapping apparatus~~ integrated circuit chip of claim 6, wherein there are at least $(2k-1)\times 2^{k-1}$ modules and at least $(2k-1)\times 2^{k-1}$ control bits and the array of modules and each control bit table has 2k-1 rows, where $p=2^k$ and $k>0$.

8. (Currently Amended) The ~~mapping apparatus~~ integrated circuit chip of claim 7, wherein the first group of modules comprises the i=1 row of the array and the second group of modules comprises the i=2k-1 row of the array.

9. (Currently Amended) The ~~mapping apparatus~~ integrated circuit chip of claim 5, wherein there are at least $(2k-1)\times 2^{k-1}$ modules and at least $(2k-1)\times 2^{k-1}$ bits, where $p=2^k$ and $k>0$.

10-20. (Canceled)

21. (New) A routing multiplexer system comprising:

n multiplexer inputs;

p multiplexer outputs based on a selected permutation of the n multiplexer inputs, where p and n are integer variables and $n \geq p$;

a plurality of modules arranged in an array of interconnected rows, each module having first and second inputs, first and second outputs and a control input and arranged to supply signals at the first and second inputs to the first and second outputs in a

direct or transposed order based on a value of a control bit at the control input, the array comprising a first row formed by a first group of p/2 of the modules of which the first and second inputs are each coupled to a respective one of the n multiplexer inputs and a last row formed by a second group of p/2 of the modules of which the first and second outputs are each coupled to a respective one of the p multiplexer outputs; and

a memory containing a plurality of control bit tables, each control bit table containing rows, each containing a plurality of control bits in an arrangement based on a respective permutation, the memory being responsive to the selected permutation to supply a j-th bit at an i-th row of a selected control bit table that corresponds to the selected permutation to the corresponding control input of the j-th module of the i-th row of the array.